DATA SHEET

PCKV857

70–190 MHz differential 1:10 clock driver

Product data
Supersedes data of 2001 Dec 03

2002 Sep 13

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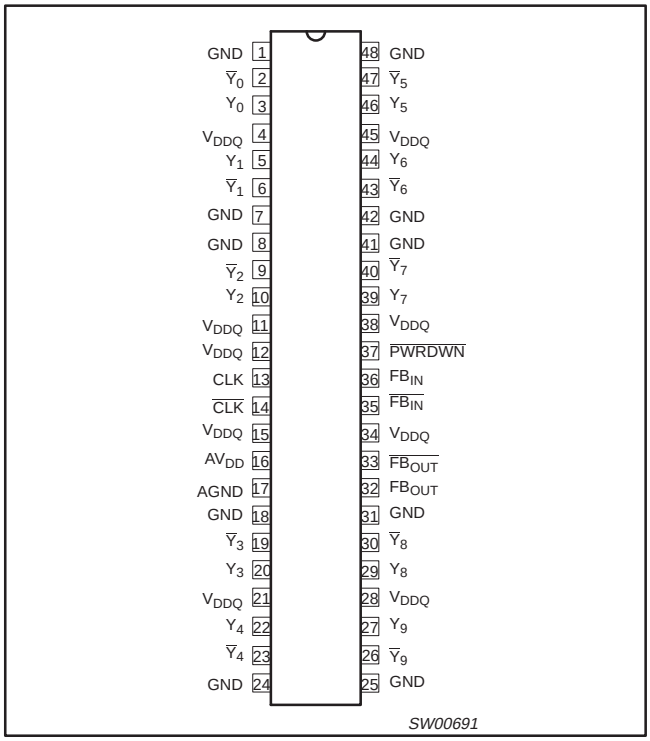
70–190 MHz differential 1:10 clock driver PCKV857

FEATURES

- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications as per JEDEC specifications
- 1-to-10 differential clock distribution
- Very low skew (< 100 ps) and jitter (< 100 ps)
- Operation from 2.2 V to 2.7 V AV_{DD} and 2.3 V to 2.7 V V_{DD}
- SSTL_2 interface clock inputs and outputs
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Full DDR solution provided when used with SSTL16877 or SSTV16857
- Designed for DDR 200 and 266 DIMM applications
- Available in TSSOP-48, TVSOP-48, and VFBGA56 (8 no connects) packages

PIN CONFIGURATION



DESCRIPTION

The PCKV857 is a high-performance, low-skew, low-jitter zero delay buffer designed for 2.5 V V_{DD} and 2.5 V AV_{DD} operation and differential data input and output levels.

The PCKV857 is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{CLK}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{Y[0:9]}$) and one differential pair feedback clock outputs (FB_{OUT}, $\overline{FB_{OUT}}$) . The clock outputs are controlled by the clock inputs (CLK, $\overline{CLK}$), the feedback clocks (FB_{IN}, $\overline{FB_{IN}}$), and the analog power input (AV_{DD}). When $\overline{PWRDWN}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{PWRDWN}$ is low, all outputs are disabled to high impedance state (3-State), and the PLL is shut down (low power mode). The device also enters the low power mode when the input frequency falls below 20 MHz. An input frequency detection circuit will detect the low frequency condition and after applying a > 20 MHz input signal, the detection circuit turns on the PLL again and enables the outputs.

When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes. The PCKV857 is also able to track spread spectrum clocking for reduced EMI.

The PCKV857 is characterized for operation from 0 to +70 °C.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic TSSOP	0 to +70 °C	PCKV857DGG	SOT362-1
48-Pin Plastic TSSOP (TVSOP)	0 to +70 °C	PCKV857DGV	SOT480-1
56-ball Plastic VFBGA[1]	0 to +70 °C	PCKV857EV	SOT702-1

NOTE:
1. 48 balls are connected, 8 balls are no-connects.

PIN DESCRIPTION

PINS	SYMBOL	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	SSTL_2 ground pins
2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 32, 33, 39, 40, 43, 44, 46, 47	Y_n, $\overline{Y}_n$, FB_{OUT}, $\overline{FB_{OUT}}$	SSTL_2 differential outputs
4, 11, 12, 15, 21, 28, 34, 38, 46	V_{DDQ}	SSTL_2 power pins
13, 14, 35, 36	CLK_{IN}, $\overline{CLK_{IN}}$, FB_{IN}, $\overline{FB_{IN}}$	SSTL_2 differential inputs
16	AV_{DD}	Analog power
17	AGND	Analog ground
37	$\overline{PWRDWN}$	Power-down control input

BALL CONFIGURATION

	1	2	3	4	5	6
A	GND	NC	NC	NC	NC	GND
B	Y_0	$\overline{Y}_0$	V_{DD}	V_{DD}	$\overline{Y}_5$	Y_5
C	$\overline{Y}_1$	Y_1	GND	GND	Y_6	$\overline{Y}_6$
D	$\overline{Y}_2$	GND	Y_2	Y_7	GND	$\overline{Y}_7$
E	V_{DD}	V_{DD}			V_{DD}	$\overline{PWRDWN}$
F	CLK	$\overline{CLK}$			$\overline{FB_{IN}}$	FB_{IN}
G	AV_{DD}	AGND	V_{DD}	V_{DD}	FB_{OUT}	$\overline{FB_{OUT}}$
H	$\overline{Y}_3$	Y_3	GND	GND	Y_8	$\overline{Y}_8$
J	Y_4	$\overline{Y}_4$	V_{DD}	V_{DD}	$\overline{Y}_9$	Y_9
K	GND	NC	NC	NC	NC	GND

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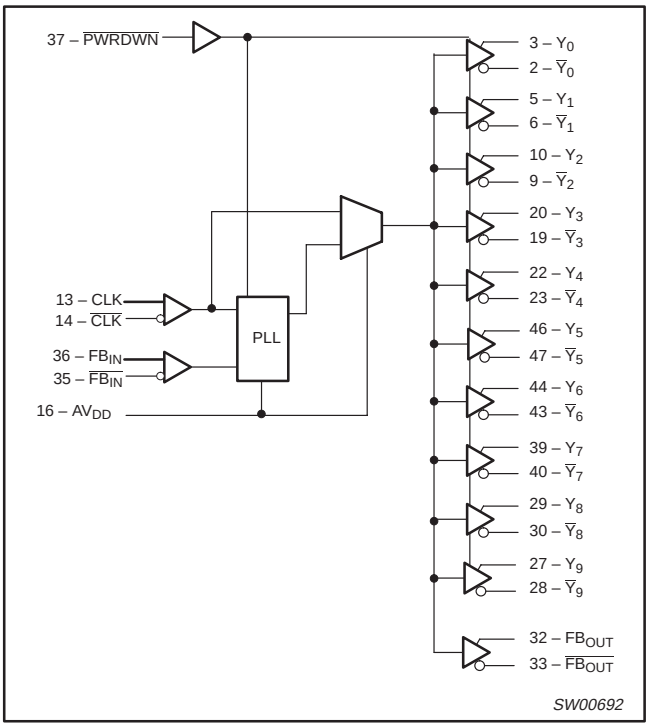
FUNCTION TABLE

INPUTS			OUTPUTS				PLL ON/OFF
$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y_n	$\overline{Y}_n$	FB_{OUT}	$\overline{FB_{OUT}}$	
L	L	H	Z	Z	Z[1]	Z[1]	OFF
L	H	L	Z	Z	Z[1]	Z[1]	OFF
H	L	H	L	H	L	H	ON
H	H	L	H	L	H	L	ON
X[2]	< 20 MHz	< 20 MHz	Z	Z	Z[1]	Z[1]	OFF

NOTES:
H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care
1. Subject to change. May cause conflict with FB_{IN} pins.
2. Additional feature that senses when the clock input is less than 20 MHz and places the part in sleep mode.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DDQ}	Supply voltage range		0.5	3.6	V
AV_{DD}	Supply voltage range		0.5	3.6	V
V_I	Input voltage range	see Notes 2 and 3	–0.5	V_{DDQ} + 0.5	V
V_O	Output voltage range	see Notes 2 and 3	–0.5	V_{DDQ} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 or V_I > V_{DDQ}	—	±50	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{DDQ}	—	±50	mA
I_O	Continuous output current	V_O = 0 to V_{DDQ}	—	±50	mA
	Continuous current to GND or V_{DDQ}		—	±100	mA
T_{stg}	Storage temperature range		–65	+150	°C

NOTES:
1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 3.6 V maximum.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER		CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
V_{DDQ}	Supply voltage range			2.3	—	2.7	V
AV_{DD}	Supply voltage range			2.2	—	2.7	V
V_{IL}	Low level input voltage	CLK, $\overline{CLK}$, FB_{IN}, $\overline{FB_{IN}}$		—	—	V_{DDQ}/2 – 0.18	V
		$\overline{PWRDWN}$		–0.3	—	0.7	
V_{IH}	High level input voltage	CLK, $\overline{CLK}$, FB_{IN}, $\overline{FB_{IN}}$		V_{DDQ}/2 + 0.18	—	—	V
		$\overline{PWRDWN}$		1.7	—	V_{DDQ} + 0.3	
	DC input signal voltage		Note 2	–0.3	—	V_{DDQ}	V
V_{ID}	DC differential input signal voltage	CLK, FB_{IN}	Note 3	0.36	—	V_{DDQ} + 0.6	V
	AC differential input signal voltage	CLK, FB_{IN}	Note 3	0.7	—	V_{DDQ} + 0.6	V
V_{OX}	Output differential cross-voltage		Note 4	V_{DDQ}/2 – 0.2	V_{DDQ}/2	V_{DDQ}/2 + 0.2	V
V_{IX}	Input differential cross-voltage		Note 4	V_{DDQ}/2 – 0.2	—	V_{DDQ}/2 + 0.2	V
I_{OH}	High-level output current			—	—	–12	mA
I_{OL}	Low-level output current			—	—	12	mA
SR	Input slew rate			1	—	4	V/ns
T_{amb}	Operating free-air temperature			0	—	70	°C

NOTES:
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IK}	Input voltage, all inputs	V_{DDQ} = 2.3 V, I_I = –18 mA	—	—	–1.2	V
V_{OH}	High-level output voltage	V_{DDQ} = min to max, I_{OH} = –1 mA	V_{DDQ} – 0.1	—	—	V
		V_{DDQ} = 2.3 V, I_{OH} = –12 mA	1.7	—	—	V
V_{OL}	Low-level output voltage	V_{DDQ} = min to max, I_{OL} = 1 mA	—	—	0.1	V
		V_{DDQ} = 2.3 V, I_{OL} = 12 mA	—	—	0.6	V
I_I	Input current	V_{DDQ} = 2.7 V, V_I = 0 V to 2.7 V	—	—	±10	µA
I_{OZ}	High-impedance-state output current	V_{DDQ} = 2.7 V, V_O = V_{DDQ} or GND	—	—	±10	µA
I_{DDPD}	Power-down current on V_{DDQ} + AV_{DD}	CLK and $\overline{CLK}$ = 0 MHz, $\overline{PWRDWN}$ = low; Σ of I_{DD} and AI_{DD}	—	30	100	µA
I_{DD}	Dynamic current on V_{DDQ}	f_O = 67 MHz to 190 MHz	—	200	300	mA
AI_{DD}	Supply current on AV_{DD}	f_O = 67 MHz to 190 MHz	—	8	10	mA
C_I	Input capacitance	V_{CC} = 2.5 V, V_I = V_{CC} or GND	2	2.8	3	pF

NOTE:
1. This is intended to operate in the SSTL_2 type IV unterminated mode without series resistors on the outputs.
2. All typical values are at respective nominal V_{DDQ}.
3. Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing.

TIMING REQUIREMENTS

Over recommended ranges of supply voltage and operating free-air temperature.

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{CK}	Operating clock frequency	60	190	MHz
	Input clock duty cycle	40	60	%
	Stabilization time[1]	100	—	µs

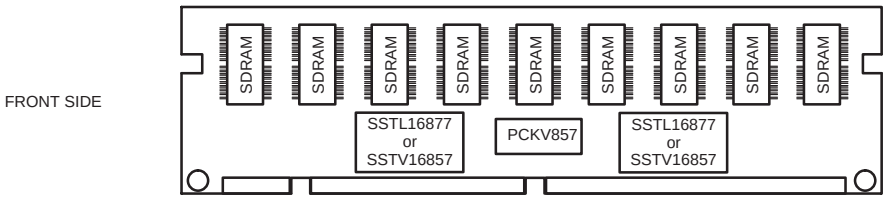
NOTE:
1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power-up.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ kΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
$t_{(O)}$	Static phase offset	Figure 1		–150	0	150	ps
$t_{SK(O)}$	Output clock skew	Figure 2		—	—	75	ps
$t_{SLR(O)}$	Output clock skew rate	Figure 3		1	—	2	V/ns
$t_{JIT(PER)}$	Jitter (period)	Figure 4	f_O = 67 MHz to 200 MHz	–75	—	75	ps
$t_{JIT(CC)}$	Jitter (cycle-to-cycle)	Figure 5	f_O = 67 MHz to 200 MHz	–75	—	75	ps
$t_{JIT(HPER)}$	Half-period jitter	Figure 6		–100	—	100	ps
t_{PLH}[1]	Low to high level propagation delay		Test mode/CLK to any output	—	3.7	—	ns
t_{PHL}[1]	High to low level propagation delay		Test mode/CLK to any output	—	3.7	—	ns

NOTE:
1. Refers to transition of noninverting output.



The PLL clock distribution device and SSTL registered drivers reduce signal loads on the memory controller and prevent timing delays and waveform distortions that would cause unreliable operation

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AC WAVEFORMS

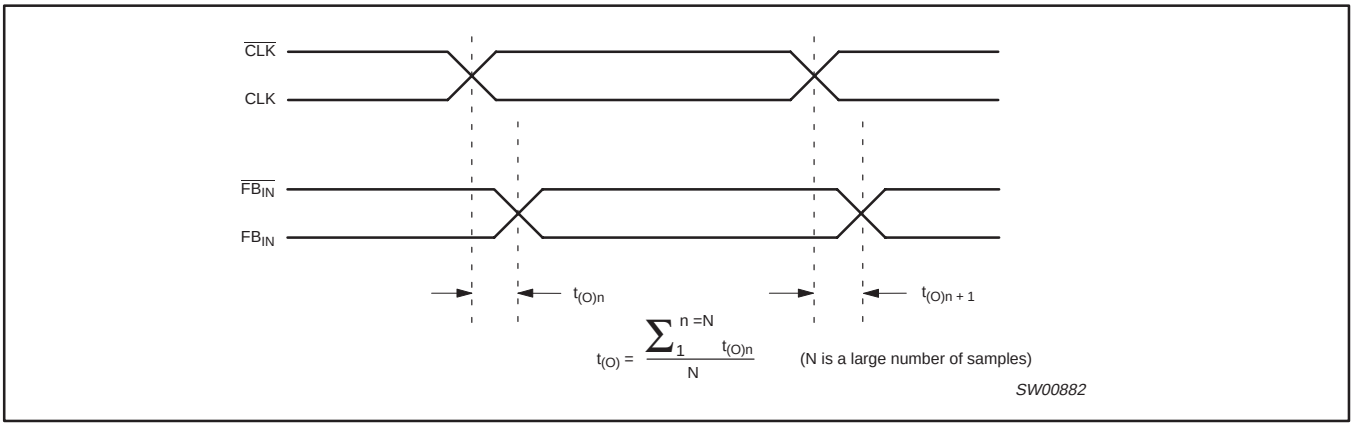


Figure 1. Static phase offset

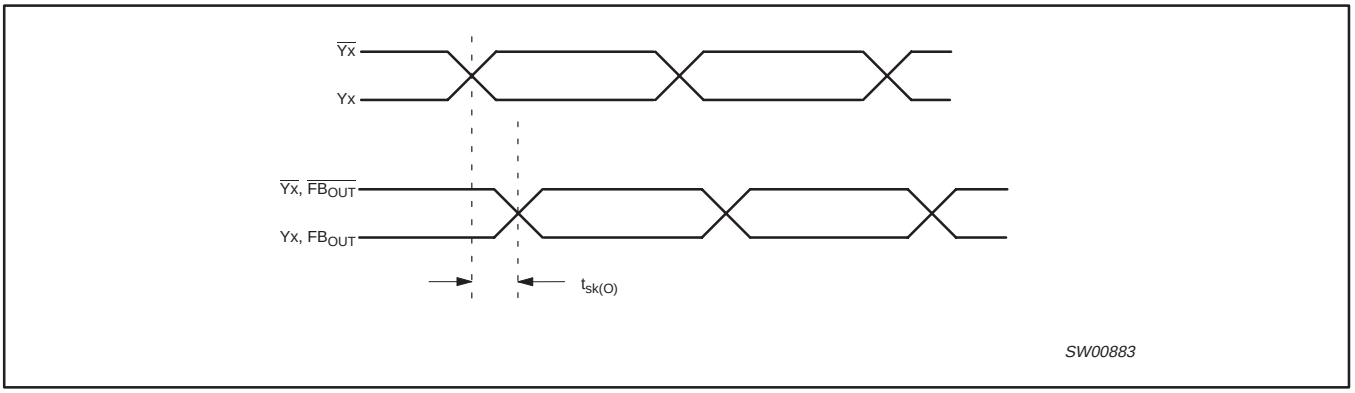


Figure 2. Output skew

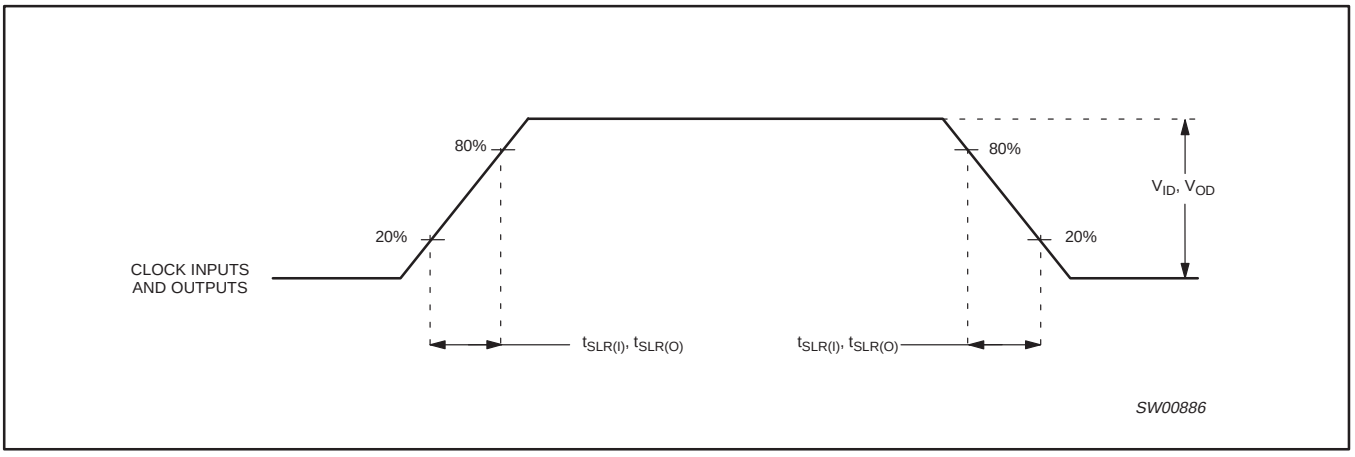


Figure 3. Input and output slew rates

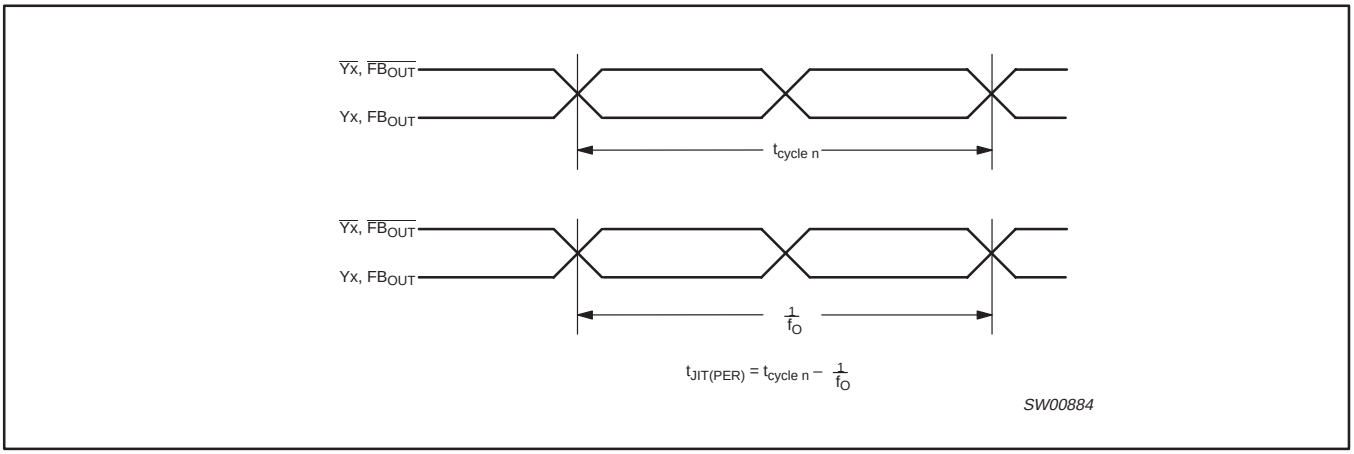


Figure 4. Period jitter

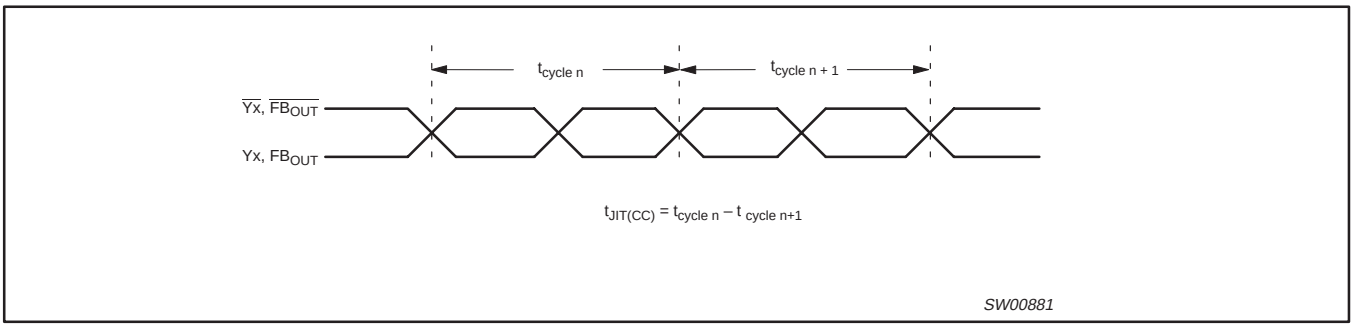


Figure 5. Cycle-to-cycle jitter

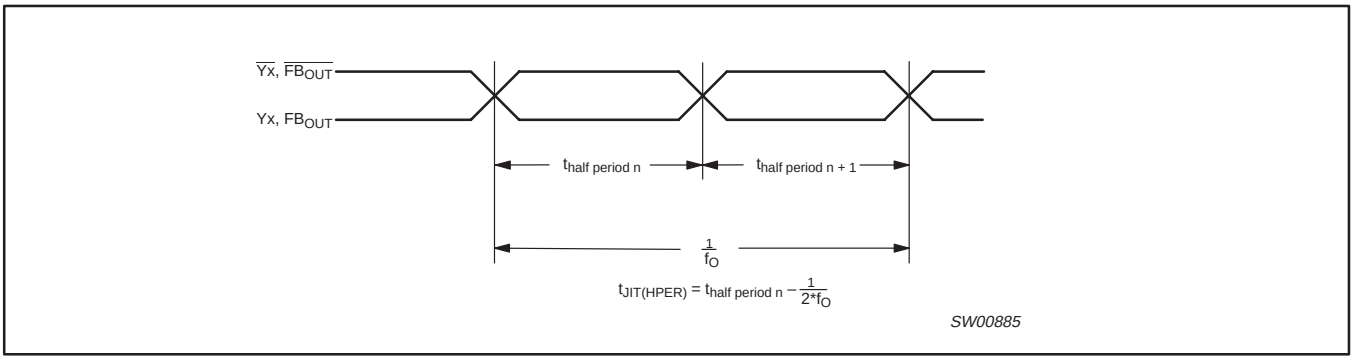


Figure 6. Half-period jitter

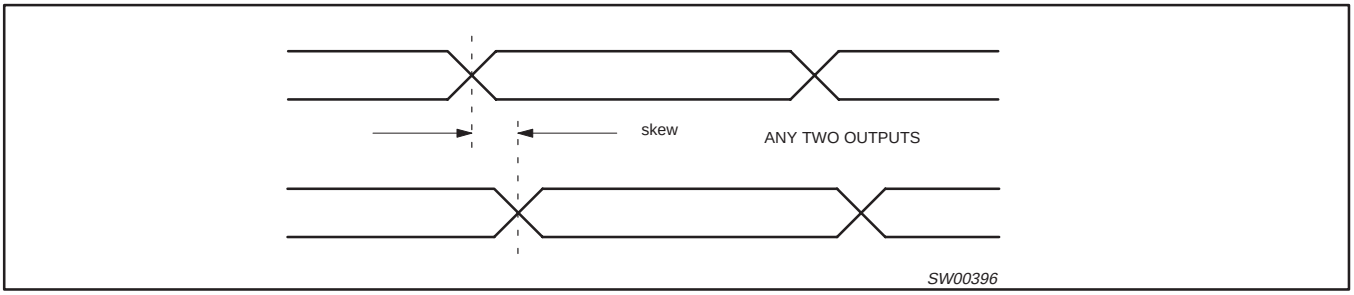


Figure 7. Skew between any two outputs.

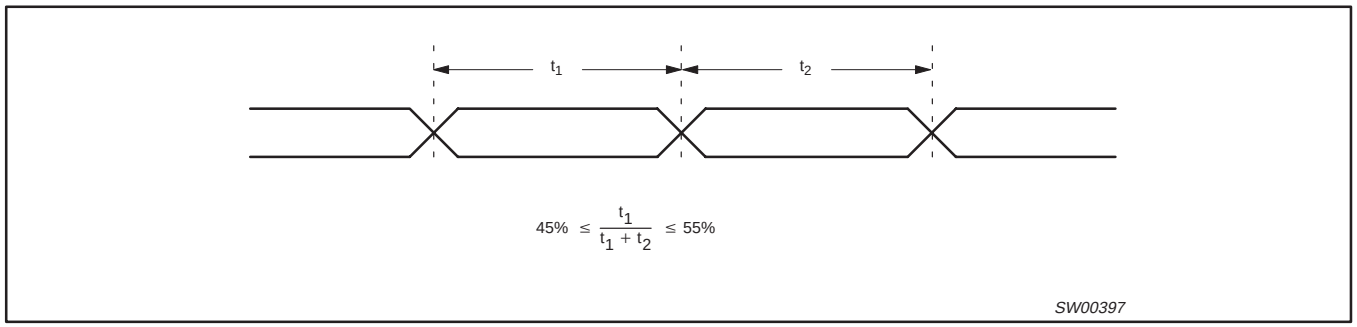


Figure 8. Duty cycle limits and measurement

TEST CIRCUIT

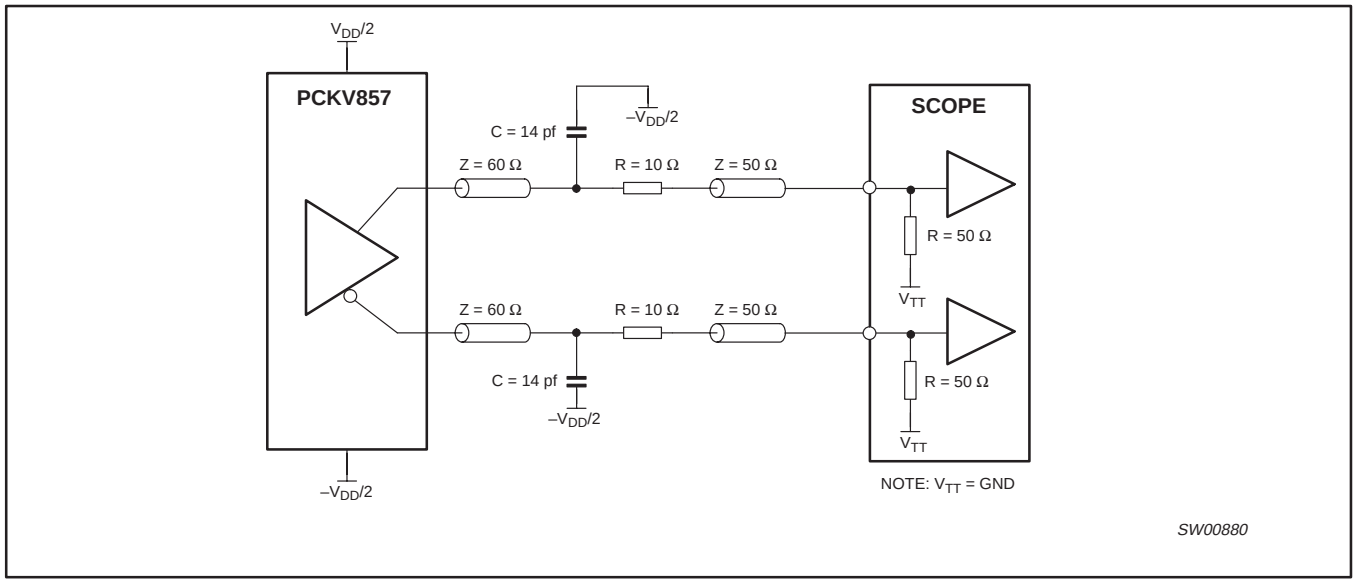
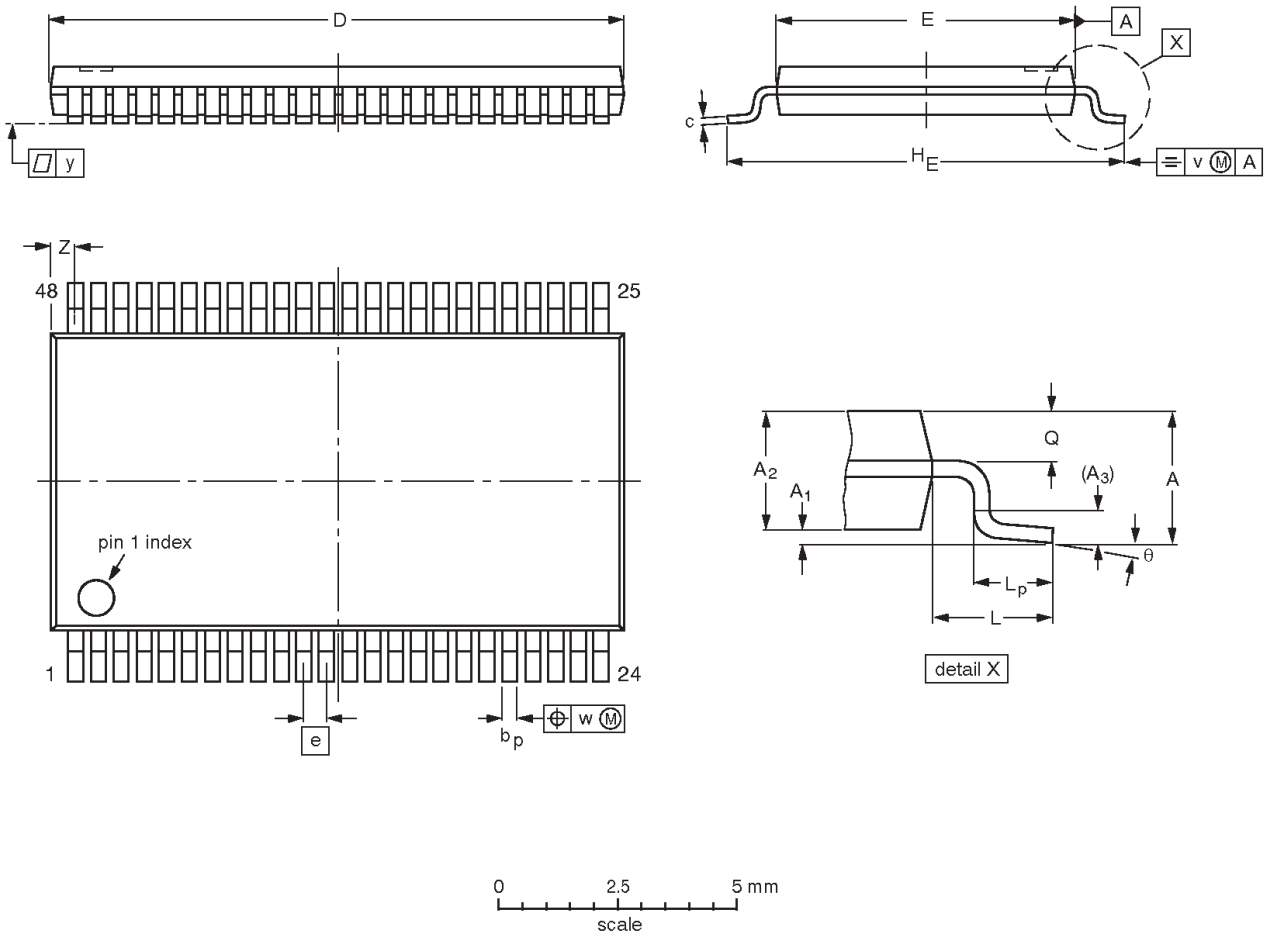


Figure 9. Output load test circuit

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1



DIMENSIONS (mm are the original dimensions).

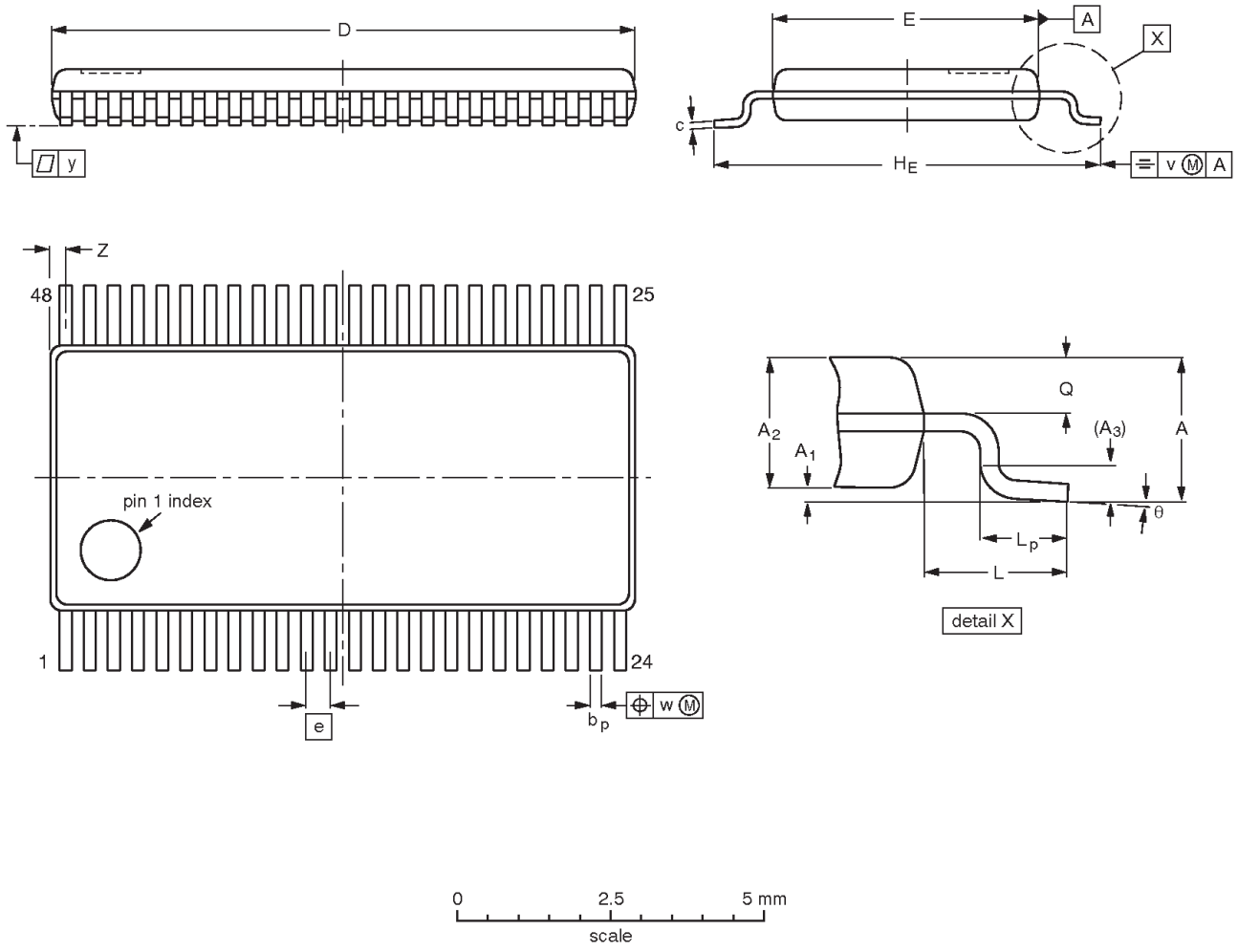
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm **SOT480-1**



DIMENSIONS (mm are the original dimensions)

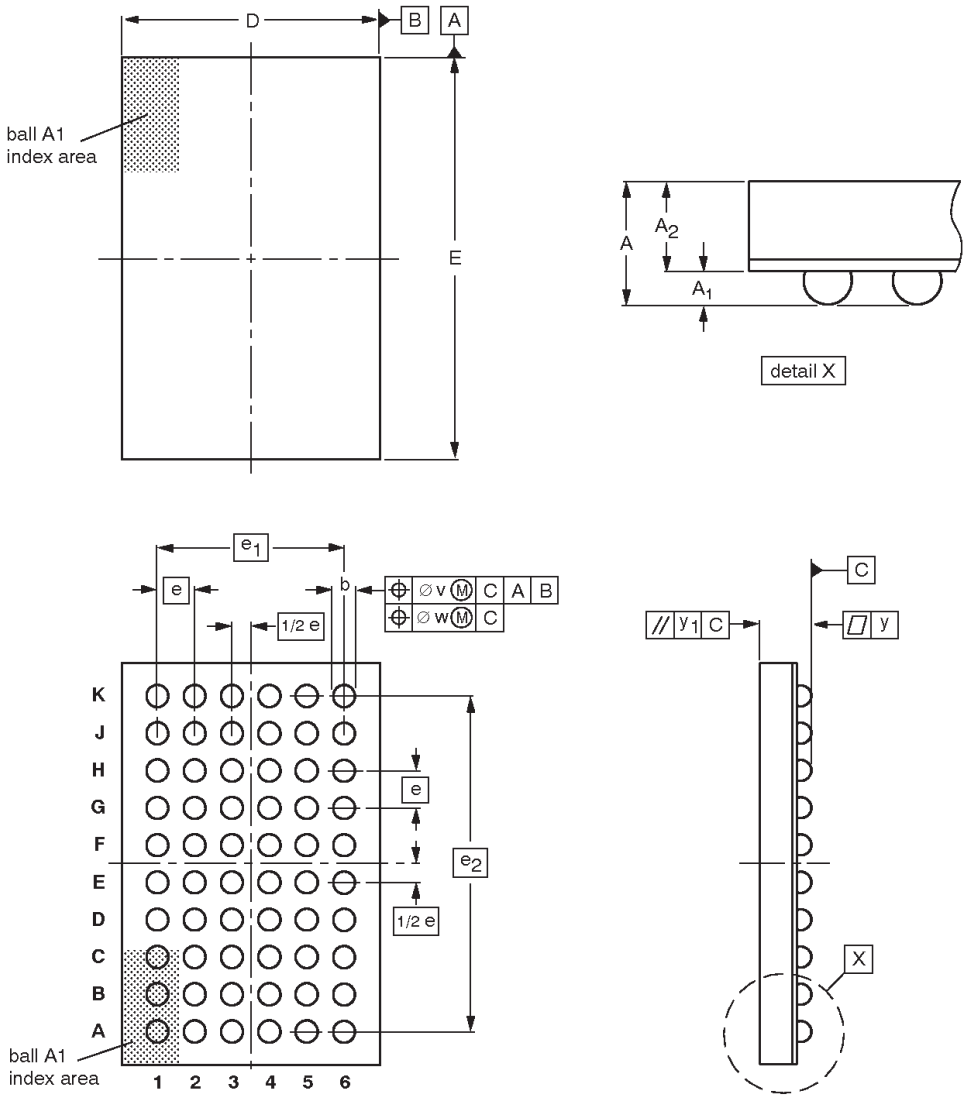
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.80 9.60	4.50 4.30	0.40	6.60 6.20	1.00	0.70 0.50	0.40 0.30	0.20	0.07	0.08	0.40 0.10	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

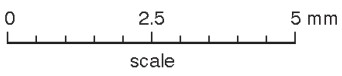
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT480-1		MO-153				~~97-03-20~~ 99-12-27

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm **SOT702-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~01-06-25~~ 02-08-08

REVISION HISTORY

Rev	Date	Description
_4	2002 Sep 06	Product data (9397 750 10343); fourth version supersedes Product data 2001 Dec 03. Engineering Change Notice 853-2242 28874 (2002 Sep 09). Modifications: Add new package option (VFBGA) to existing product data sheet.
_3	2001 Dec 03	Product data (9397 750 09244); third version

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued datasheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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